A 12 Switch Zero-Inductor Voltage Converter Topology For Next Generation Datacenters

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Abstract—**Advancements in datacenter power architecture has led to 48V to 12V intermediate bus converters becoming a resurgent area of research interested. The 48 volt server architecture, proposed by companies such as Google, can offer significant benefits. This higher voltage reduces the distribution losses by 4x as compared with a 12V distribution, as well ad reducing the power conversion losses at the building level. However, increasing this server rack voltage to 48 volts presents a challenge when converting down to point of load voltages using conventional topologies. The Zero Inductor-Voltage converter that can achieve up to 2.5kW/in^3 power density for 70A/12V output. The full load efficiency was measured to be 97.2% with a peak efficiency of 99.1%. This represents the highest efficiency and power density yet demonstrated. The design of the converter is also relatively straightforward as there is no need for active current sharing control, and the converter does not utilize resonant components.**

Keywords—DC-DC Converter, Datacenter, Intermediate Bus

I. INTRODUCTION

The introduction of the 48V server power architecture, proposed and implemented by companies such as Google, has led to a resurgence of research interest in Switched Capacitor (SC) converters. These SC converters are often used as a so-called intermediate bus converter, where the 48V supplied to the server rack is converter down to some lower voltage (such as 12V) before being converter to the POL voltage in a two-stage conversion process. SC converters are attractive for this application as they can offer substantially higher power density than PWM-based converters owing to their reduced reliance on magnetic components. Additionally, one of the major drawbacks of the SC converter, namely that they operate optimally at a fixed integer voltage step-down ratio is not a drawback in an intermediate bus application. The mechanism of charge redistribution loss [1] in SC converters, however, reduce the power density and efficiency achieved in practice as large flying capacitors or higher switching frequencies must be utilized reducing the efficiency and power density of the converter. One way to avoid this charge redistribution loss is to add an inductive element to the SC topology. As outlined in [2] there are several critical issues with many of these topologies that make them unsuitable for use in practical industrial applications. Firstly, the sensitivity of the converter to

manufacturing tolerances and component non-idealities is a concern for sensitive resonant based designs. Second, optimal utilization of the switching devices should be achieved to reduce the RMS current stress as the conduction loss is a dominant source of loss for many of these topologies. Finally, complex control or the inability to easily parallel multiple phases makes it extremely difficult to scale the topologies for differing power levels and to create a modular design. The results presented are an extension and improvement on the 12-Switch ZIV converter [3]. A multiphase design for the ZIV converter is presented in this work as the paralleling of multiple phases is a very useful technique enabling more modular designs and the ability to scale to different power levels.
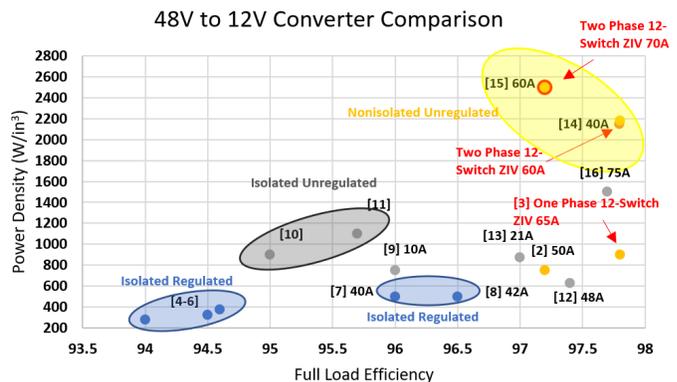
Fig. 1 Comparison of Converter Topologies for 48V to 12V Conversion Referenced From [17]

The ZIV converter topology is a nonisolated unregulated topology. Isolation and regulation are not requirements in an intermediate bus application, and as Figure 1 shows, utilizing nonisolated unregulated topologies can offer substantial improvements in both efficiency and power density. An example of this is the cascaded resonant converter presented in [14]. As a nonisolated, unregulated topology this cascaded resonant converter design achieves a 12V/40A power density of 2.2kW/in^3 and the efficiency under this full load condition is 97.8%. A second cascaded resonant converter design [15] further increased the full load to 12V/60A. At this power level

the power density for the second design was 2.5kW/in³ with a 12V/60A efficiency of 97.2%. The Two-Phase 12-Switch ZIV converter prototype presented here achieves a full load 12V 70A efficiency of 97.2% and a power density of 2.5kW/in³. This represents the best overall performance level yet demonstrated for 48V to 12V conversion.

II. EQUIVALENT CIRCUIT ANALYSIS

A. Steady-State Analysis

The 12-Switch ZIV Converter topology is presented in Figure 2. Figure 3 shows the associated PWM gate diagram. The operation of the 12-Switch ZIV converter can be understood by examining the equivalent circuits of each switching state. The equivalent circuit for State A (as labelled in Figure 3) is shown in Figure 4.
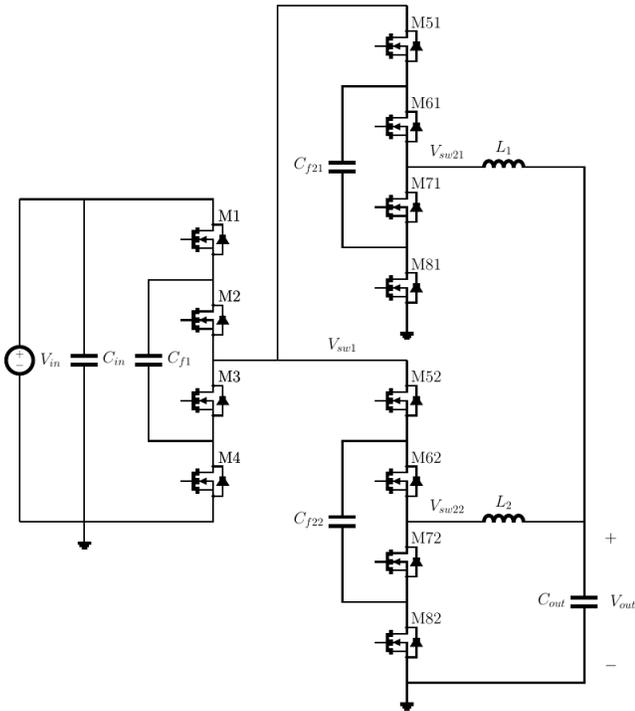
Fig. 2 One Phase of the 12-Switch ZIV Converter
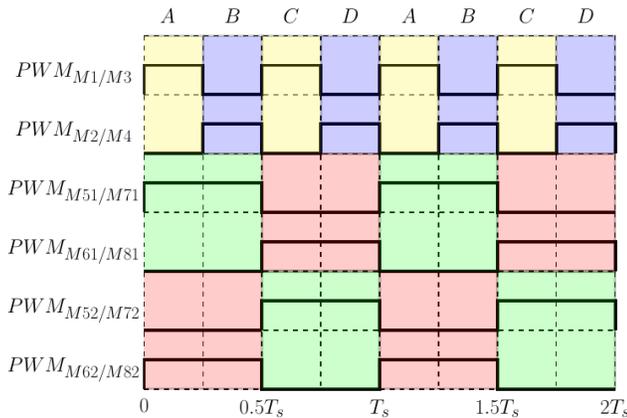
Fig. 3 12-Switch ZIV Converter PWM Gate Timing Diagram
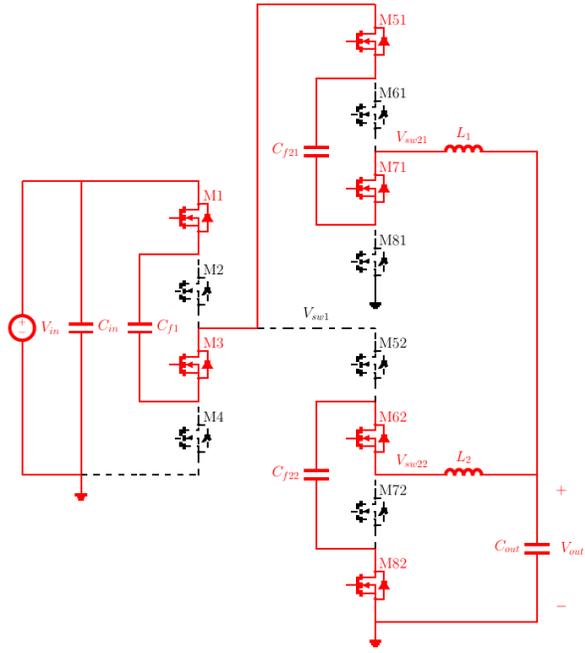
Fig. 4 12-Switch ZIV Converter State A Equivalent Circuit
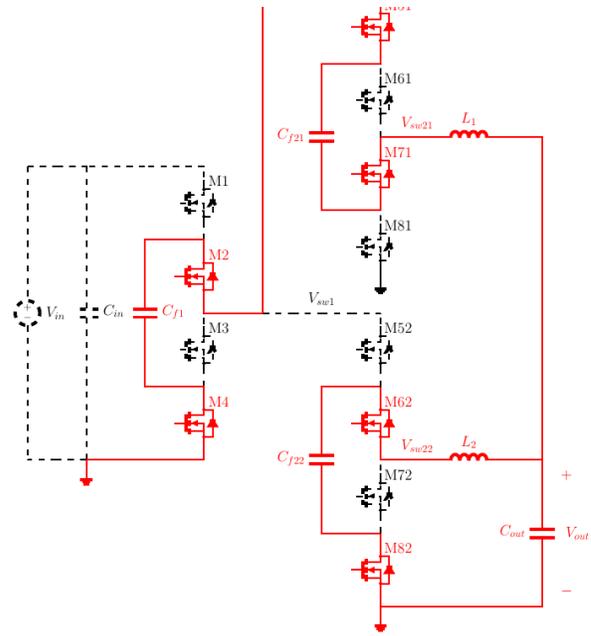
Fig. 5 12-Switch ZIV Converter State B Equivalent Circuit

The equivalent circuit for State B (as labelled in Figure 5) is shown in Figure 5. It should be noted that States C and D are simply mirrored to State A and B, with M52 and M72 being turned on instead of M51 and M71, and M61 and M81 being turned on instead of M62 and M82 as shown in Figure 3. Therefore, for brevity the equivalent circuits for these states are not shown.

144

In order to understand the 4:1 step down ratio provided by this converter topology the inductor voltage can be analyzed in the steady state. Let V_{L1A} be the voltage across the inductor L_1 in State A, V_{L1B} is the voltage across L_1 in State B, V_{L1CD} is the voltage across the inductor L_1 in both States C and D. Note that in States C and D the MOSFET M51 will be turned off, disconnecting L_1 from the input stage, and therefore from the perspective of the inductor L_1 States C and D are equivalent and can be analyzed together. V_{Cf1-A} and V_{Cf21-A} are the two flying capacitor voltages in State A, V_{Cf1-B} and V_{Cf21-B} are the two flying capacitor voltages in State B, and $V_{Cf21-CD}$ is the second flying capacitor voltage in States C and D. Note once again because M51 will be turned off in States C and D these states can be analyzed together.

$$V_{L1A} = V_{in} - V_{cf1-A} - V_{cf21-A} - V_{out} \qquad \text{State A (1)}$$

$$V_{L1B} = V_{cf1-B} - V_{cf21-B} - V_{out} \qquad \text{State B (2)}$$

$$V_{L1CD} = V_{cf21-CD} - V_{out} \qquad \text{State C and D (3)}$$

From the PWM gate diagram presented in Figure 3, State A is active from 0-0.25T$_s$, State B is active from 0.25T$_s$-0.5T$_s$, State C is active from 0.5T$_s$-0.75T$_s$ and State D is active fro, 0.75T$_s$-T$_s$. Thus the average inductor voltage over one switching cycle can be expressed as:

$$V_{L1} = \frac{V_{L1A}}{4} + \frac{V_{L1B}}{4} + \frac{V_{L1CD}}{2} \qquad (4)$$

Note that by definition under steady state operation the capacitor voltage balance will be maintained. This means that the average voltage of C_{f1} in State A must be equal to the average voltage of C_{f1} for State B, as C_{f1} is charged for 25% of the switching cycle in State A, discharged for 25% of the switching cycle in State B, and is disconnected from the output inductor in States C and D:

$$V_{cf1-A} = V_{cf1-B} \qquad (5)$$

For C_{f21} the average voltage of C_{f21} across both States A and B must be equal to the average voltage of C_{f21} across State C and D. This is because C_{f21} is charged for 25% of the switching cycle in State A, continues to be charged for 25% of switching cycle in State B, and then is discharged for the remaining 50% of the switching cycle in States C and D:

$$\frac{V_{cf21-A} + V_{cf21-B}}{2} = V_{cf21-CD} \qquad (6)$$

Substituting equations (1) (2) and (3) into equation (4) gives the expanded form:

$$V_{L1} = \frac{V_{in}}{4} - \left(\frac{V_{cf1-A}}{4} - \frac{V_{cf1-B}}{4}\right) - \left(\frac{V_{cf21-A}}{4} + \frac{V_{cf21-B}}{4} - \frac{V_{cf2-CD}}{2}\right) - V_{out} \quad (7)$$

$$V_{L1} = \frac{V_{in}}{4} - (0) - (0) - V_{out} = 0 \qquad (8)$$

Under steady state operation the average inductor voltage across one switching cycle must be zero, and utilizing the equivalencies given in (5) and (6) the capacitor voltage terms cancel out as shown in (8) leaving:

$$V_{out} = \frac{V_{in}}{4} \qquad (9)$$

By noting that the States C and D are mirrored to States A and B, it therefore follows that the analysis above also holds for L_2. Thus the 12-Switch ZIV converter provides a fixed 4:1 stepdown ratio under steady-state operation.

B. Zero Inductor-Voltage Property

A key advantage of this topology, the zero inductor-voltage operation for which it is named, can be seen by examining the output voltage of the converter before the inductor and capacitor output filter (V_{sw21}). Note that the first flying capacitor is charged to 1/2 of the input voltage nominally, and both of the second stage flying capacitors are charged to 1/4 of the input voltage nominally. These capacitor voltages can be expressed as a nominal DC value, summed with a ripple voltage. For simplicity and consistency with previous analysis only the "phase" consisting of M1-M4 and M51-M81 will be analyzed with the understanding that the second phase of M52-M82 has equivalent mirrored operation.

$$V_{Cf1} = \frac{V_{in}}{2} + v_{Cf1rip} \qquad (10)$$

$$V_{Cf21} = \frac{V_{in}}{4} + v_{Cf21rip} \qquad (11)$$

For State A:

$$v_{sw2} = V_{in} - v_{cf1} - v_{cf21} \qquad (12.1)$$

$$v_{sw2} = V_{in} - \frac{V_{in}}{2} - \frac{V_{in}}{4} - v_{cf1rip} - v_{cf21rip} \qquad (12.2)$$

$$v_{sw2} = \frac{V_{in}}{4} - v_{cf1rip} - v_{cf21rip} \qquad (12.3)$$

For State B:

$$v_{sw2} = v_{cf1} - v_{cf21} \qquad (13.1)$$

$$v_{sw2} = \frac{V_{in}}{2} - \frac{V_{in}}{4} + v_{cf1rip} - v_{cf21rip} \qquad (13.2)$$

$$v_{sw2} = \frac{V_{in}}{4} + v_{cf1rip} - v_{cf21rip} \qquad (13.3)$$

For State C and D:

$$v_{sw2} = v_{cf21} \qquad (14.1)$$

$$v_{sw2} = \frac{V_{in}}{4} + v_{cf21rip} \qquad (14.2)$$

In each state A-D, the voltage at v_{sw21} is equal to $1/4V_{in}$ plus the capacitor ripple voltage. The inductor voltage will be equal to V_{sw2} minus the output voltage. As the output voltage is equal to $1/4V_{in}$ it is then clear that the inductor sees only the capacitor ripple voltage. This means the inductor voltage is independent of the input and output voltage level. Therefore, a very small inductor can be used to achieve acceptable inductor ripple. The low voltage stress means that very small inductors, as small as 200nH, can be utilized even with switching frequencies below 100kHz.

145

III. SIMULATION RESULTS

A. Key Operating Waveforms

Simulation waveforms for a 12-Switch ZIV converter design are presented in this section. The selected parameters for simulation are shown in Table 1. Note that the circuit deadtime is not included in the simulation results. As will be shown in the loss breakdown of this section the deadtime has negligible impact on the overall circuit performance.

Table 1 Simulation Parameters

Switching Frequency	60kHz (120kHz M1-M4)
Input Voltage	48V
Output Voltage	12V
Load Current	30A
Inductor (L_1 and L_2) Value	200nH
C_{f1} Value	60µF
C_{f21} and C_{f22} Values	160µF

Figure 6 shows the input voltage, V_{sw1} voltage, and output voltage for the circuit. This demonstrates the 4:1 step-down achieved by the topology.
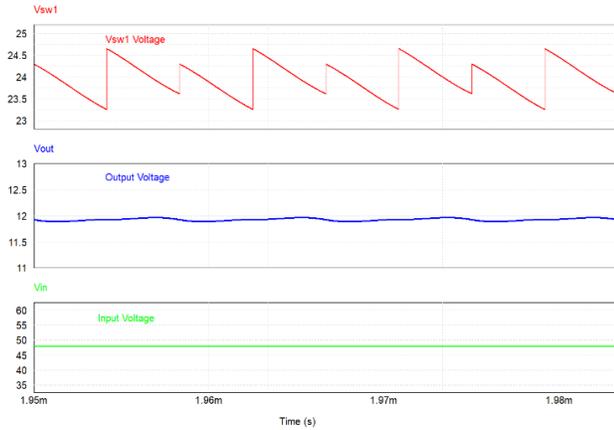
Fig 6. Input Voltage, V_{sw1} Voltage, Output Voltage Waveforms

The output voltage of each phase of the converter, at V_{sw21} and V_{sw22}, as well as the filtered output voltage is presented in Figure 7. This figure demonstrates the key advantage of the topology, namely the "zero inductor-voltage" is maintained in this two-phase 12-Switch topology.

The inductor current waveforms are shown in Figure 8. The inductor voltages for L_1, and L_2 along with the labelling of States A, B, C and D (as per Figure 3) is shown in Figure 9.
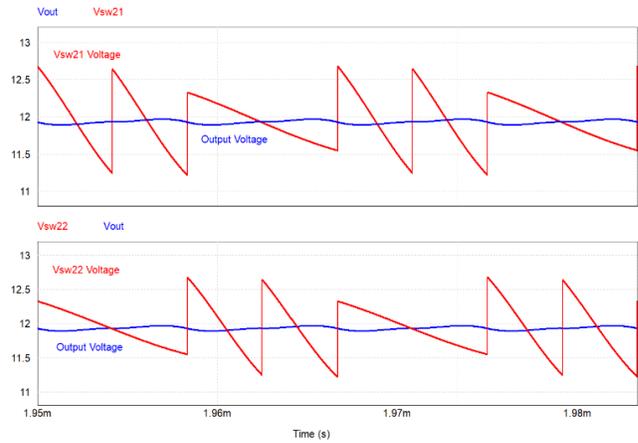
Fig. 7 V_{sw21}, V_{sw22} and Output Voltage Waveforms
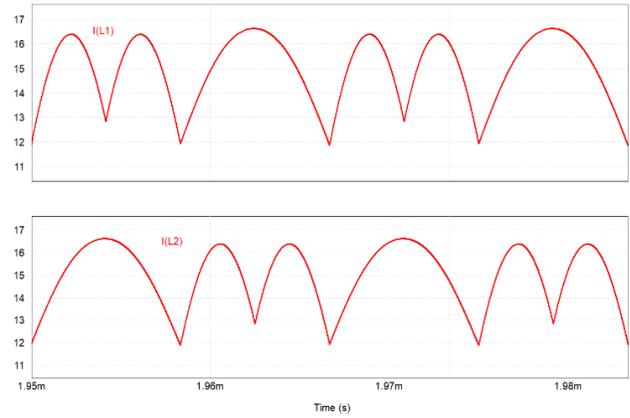
Fig 8. Inductor Current Waveforms
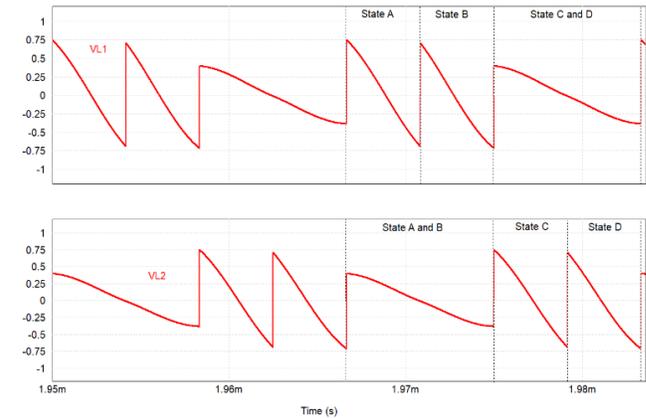
Fig 9. Inductor Voltage Waveforms

B. Loss Analysis

The 12-Switch ZIV converter presented in [3] utilized a single-phase design. However, significant improvements in terms of both power density and efficiency are possible by utilizing a multi-phase design as will be shown in the experimental results section. The loss breakdown for a Two-Phase 12-Switch ZIV converter operating at a full 70A load,

146

utilizing the components outlined in Table 2. Notably, as compared with a single-phase 12-Switch ZIV converter the input capacitor loss is, in theory, eliminated. Despite being a hard-switched topology for the ZIV converter over 85% of the total loss at full load is conduction loss. This makes multiphase designs particularly attractive as by utilizing multiple phases the conduction loss is significantly reduced.

The diode loss represents the loss associated with the deadtime in the circuit. As it is only 0.5% of the total loss, the effect of the short deadtime on the circuit operation is negligible.

Fig. 10 Two-Phase 12-Switch ZIV Converter Loss Breakdown at 70A Load

C. Current Sharing

Utilizing multiple phases operating in parallel is a very attractive option in conduction loss dominated converters to allow for scalability to differing power levels. The primarily challenge with paralleling multiple phases is ensuring that the load current is shared approximately equally between the phases. In an unregulated converter it is highly desirable to achieve this current sharing passively, which is possible by taking advantage of the droop characteristic of the output voltage. In theory the ZIV converter will output 4:1 voltage stepdown. In practice the output voltage will always be lower than this due to the voltage drop of the individual converter components as well as the cicuit board itself. If these resistances are lumped together as a single equivalent resistance then the output voltage of the converter is given by (15).

$$V_{out} = V_{out\_NL} - I_{out}R_{out} \qquad (15)$$

The output voltage of the ZIV converter as a function of load current is presented in Figure 11 based on a simulation using resistance parameters (ESR, $R_{ds(on)}$, winding resistance) approximately equivalent to the components used in the experimental prototype outlined in Table 2. For these parameters the R_{out} is approximately 10mΩ for each phase, or approximately 5mΩ for the two phases operating in parallel. The output voltage node is shared between the paralleled phases of the converter

and this means that all phases of the converter will be outputting the same output voltage.

In a two-phase ZIV converter let R_{out1} and R_{out2} be the lump resistance of all the series components in each phase of the ZIV converter connected in parallel. Then the current sharing is given by:

$$I_{out1} = I_{out}\frac{R_{out2}}{R_{out1} + R_{out2}} \qquad (16)$$

$$I_{out2} = I_{out}\frac{R_{out1}}{R_{out1} + R_{out2}} \qquad (17)$$

Fig. 11 Two-Phase ZIV Converter Modelled Output Voltage Characteristic
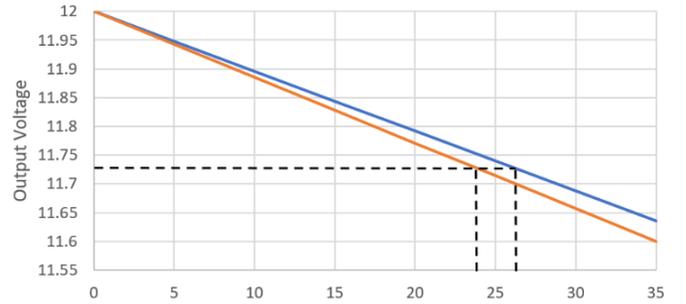
Fig. 12 Two-Phase ZIV Converter Per-Phase Output Voltage with 10% Equivalent Resistance Mis-Match

Figure 12 demonstrates a case where the resistance value of phase 2 (comprised primarily of the MOSFET $R_{ds(on)}$ and capacitor ESR) is 10% higher than the lump resistance of phase 1. Note that in Figure 12 the output current is give as the per-phase value, therefore 35A per phase current would represent the total full load current of 70A. The calculation below is performed for a load current of 50A. The current will share according to the equations:

$$I_{ph1} = 26.2A = 25A + 4.8\% \qquad (18)$$
$$I_{ph2} = 23.8A = 25A - 4.8\% \qquad (19)$$

Under this modelled operating condition of 50A load the output voltage of the converter will be 11.73V. Phase 1 of the converter will carry 26.2A of the load current, and phase 2 of the converter will carry 23.8A of the load current. As

147

demonstrated by this example the current sharing achieved with the droop sharing technique will not be exactly perfect. In the practical converter the manufacturing tolerances of the components will result in some small per-phase current mismatch however as demonstrated by the experimental results of this paper as well as the analysis presented the difference in phase currents can be kept relatively small with no additional control.

In addition to the output voltage droop characteristic the $R_{ds(ON)}$ of the silicon MOSFETs will increase with the converter temperature. If the current is imbalanced this temperature characteristic will also help to improve the current sharing of the converter as the on-resistance of the MOSFET can increase by more than 1.5X based on the device temperature, helping to offset the difference in phase resistance.

IV. EXPERIMENTAL RESULTS

This experimental results section focuses on a Two-Phase design of the 12-Switch ZIV converter. While the single-phase design was intended to verify the functionality of the topology, the Two-Phase design allows for significant power density improvements to be made. Due to interleaving, the input capacitor can be almost entirely eliminated, and by utilizing multiple phases much smaller MOSFET packages can be used. The flying capacitor size can also be substantially reduced as compared with the previous single-phase design.

Table 2 Two-Phase Experimental Prototype Components

Input Voltage	40V-60V
C_{in}	1x4.7µF 100V 1206
M1-M4	Infineon BSZ025N04LS (40V, 2.5mΩ)
C_{f1}	5x10µF 50V 1206 (top) 5x10µF 35V 0805 (bottom)
M51-M82	Infineon BSZ017NE2LS5I (25V, 1.7mΩ)
C_{f2} and C_{f3}	3x47µF 25V 1210 (top) 4x10µF 35V 0805 (bottom)
C_{out}	3x47µF 25V 1210
L_1 and L_2	Coilcraft XEL4030-201 (200nH, 22A)
Switching Frequency	60kHz (120kHz M1-M4)

Table 2 shows the key components used in the two-phase experimental prototype. One phase of the converter measures 1" long, 0.75" wide with an overall height of 0.226" (including the inductor height of 0.126", board thickness of 0.06" and bottom side driver height of 0.04"). For 12V/70A output the power density of the ZIV converter is thus 2.5kW/in^3. The single phase 12-Switch ZIV converter design previously demonstrated achieved of approximately 900W/in^3. The key driving factors for this massive improvement in the multi-phase design are the use of smaller MOSFETs, the reduction of the input capacitor, the reduction of inductor size, and reduction in flying capacitor size. The input capacitor can be reduced from a 70µF capacitor bank to only 4.7µF due to the nearly 100% interleaving of the multi-phase design. The smaller MOSFETs, capacitors and inductors have a higher equivalent resistance, however, as the current is shared between two phases the

overall conduction loss is reduced compared to the single phase design.
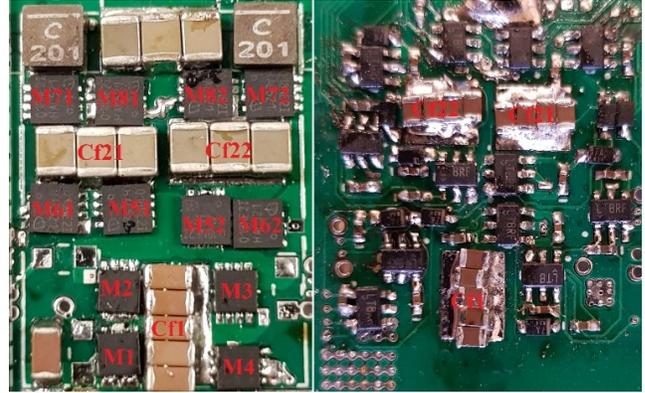
Fig. 13 Top View (Left) and Bottom View (Right) For A Single Phase of Two-Phase ZIV Converter Prototype (1"x0.75"x0.226")

While a two-phase design is demonstrated here, scalability to higher power levels may demand more than two phases be used in parallel. In this case it should be noted that an even number of phases should be used to maintain input capacitor interleaving.

Figure 14 presents some of the key operating waveforms for one phase of the converter for 48 volt input with 50A load current. CH1 shows the output voltage, CH2 shows the ripple voltage of the first stage flying capacitor, CH3 shows the ripple voltage of one of the second stage flying capacitors, and CH4 shows the V_{sw21} voltage. It should be noted that the inductor sees only the capacitor ripple current as the voltage across the inductor. This is the "zero inductor-voltage" property for which the converter family is named, and this allows the small 200nH inductor to be used in this prototype design despite the switching frequency of only 60kHz.

The negative voltage spikes seen on V_{sw21} are due to the deadtime added in the practical circuit. During the deadtime the low-side MOSFETs will reverse conduct, however, this deadtime is by design very short and the overall impact on the circuit operation and output voltage is negligible.
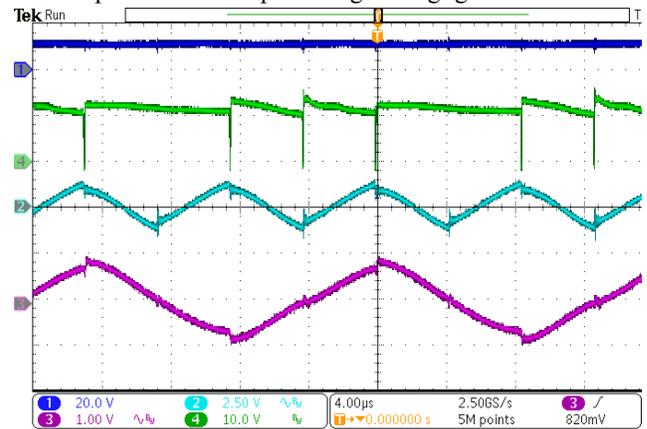
Fig. 14 Prototype Waveforms of V_{out}, V_{sw21} and Flying Capacitor Ripple for 12V/50A Load

148

Figure 15 shows the output voltage of the ZIV converter prototype as a function of load current.

ZIV Converter Output Voltage
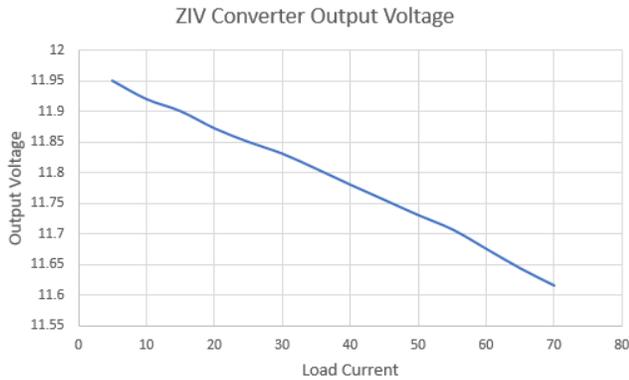
Fig. 15 Measured Output Voltage as a Function of Load Current (48V input)

Figure 16 shows a thermal image of the prototype operating at 12V/40A load with no fan cooling.
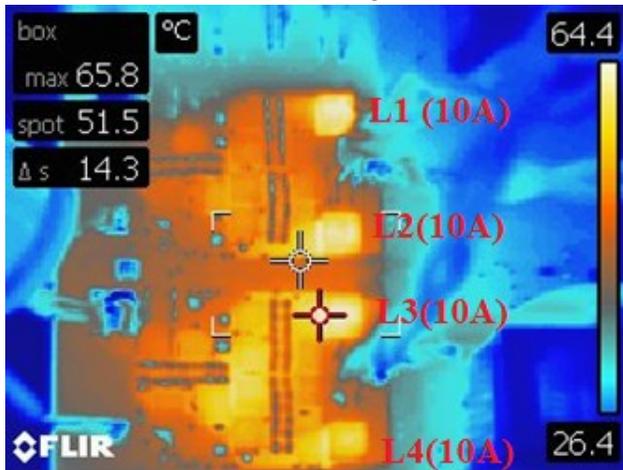
Fig. 16 40A Load No Fan Cooling

The prototype achieves even thermal performance, with the hottest components under this operating condition being the inductors each carrying a per-phase current of approximately 10A. This illustrates that the two-phase ZIV converter can passively share current with no additional control required.

The experimental prototype presented in this paper has a maximum output current of 70A. Under the full load condition the efficiency of the converter (including gate drive loss) is 97.2%. The casecaded resonant converter [15] also achieves a full load efficiency of 97.2% but for 60A load current. At 60A load current the ZIV converter prototype efficiency was measured to be 97.8%.

The volume of one phase of the ZIV converter design is approximately 0.17in^3. At the maximum output current of 70A, for 12V output, this gives a power density of 2500W/in^3 which matches the power density of [15] while achieving higher full load current and efficiency. This ZIV converter prototype is designed to handle input voltages up to 60V, and the efficiency for both 48V input and 60V input are presented in Figure 17.

The measurements were taken using a Keithley 2700 digital multimeter, and Reidon RSN series (0.1% error) current shunts.

It should be noted that the maximum load current of 70A is selected based on thermal considerations. With better cooling, such as through the use of a heatsink, or more powerful fan, then the converter design can output higher current. The saturation current of the selected inductors is 22A, meaning this Two-Phase design could theoretically output up to 88A (just over 1kW output power) with sufficient cooling.
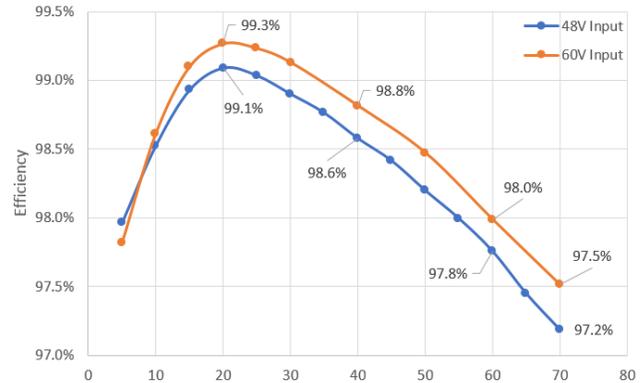
Fig. 17 Measured Efficiency for Two-Phase Experimental Prototype Including Gate Drive Loss

V. CONCLUSION

While many of the existing intermediate bus converters, especially those based on SC converter topologies, have critical issues that presents their widespread adoption in industry the ZIV converter family avoids many of these drawbacks. The ZIV converter has low sensitivity to component-to-component variation as it does not rely on any sensitive resonant design. As demonstrated by the theoretical analysis and experimental results the 12-Switch ZIV converter can achieve multiphase current sharing passively, allowing for scalability to differing power levels to be achieved with a modular design. As the conduction loss is the primary source of loss in the ZIV converter a multiphase design also allows for significant power density and/or efficiency improvements to be made over a single-phase design. This Two-Phase ZIV converter design achieved 3x higher power density than a previous single phase design for similar output power.

The ZIV converter design, as shown in Figure 1, equals the highest power density yet demonstrated for 48V to 12V conversion while also achieving higher efficiency at a higher output current level.

The reason for this efficiency improvement can be seen by examining the relative current and voltage stresses for the components in the 12-Switch ZIV converter as compared with the cascaded resonant converter. Both converter topologies require 3 capacitors and 2 inductors per phase. In the cascaded resonant converter the voltage stress for two of these capacitors is $1/2V_{in}$ and for the third it is $1/4V_{in}$. In the 12-Switch ZIV converter only one capacitor sees $1/2V_{in}$ stress and the other two see $1/4V_{in}$. Similarly, the current stress of the second stage

149

flying capacitor in the cascaded resonant converter will be equal to the full load current, while in the 12-Switch ZIV converter both second stage flying capacitors C_{f21} and C_{f22} carry only $1/2I_{out}$. In the 12-Switch ZIV converter both of the inductors carry $1/2I_{out}$ as their RMS current. In the cascaded resonant converter, one inductor will carry $1/2I_{out}$ and one inductor will carry the full load current. The ZIV converter requires 12 switches per phase instead of 8, however, all 12 switches in the ZIV converter carry $1/2I_{out}$ when switched on. In the cascaded resonant converter only 8 switches are required, but while 4 of these switches will carry $1/2I_{out}$, 4 of the switches will carry the full load current. This means that the overall conduction loss, the dominant source of loss in the converter, is reduced. While the cascaded resonant converter eliminates switching loss due to the resonant operation, the conduction loss dominates the overall loss and therefore the reduced current stress of the ZIV converter allows for higher efficiency to be achieved without needing a resonant based design.

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